Supertex inc.

Preliminary

High Voltage Isolated MOSFET Driver

Ordering Information

Package Options	
8-Pin Narrow Body SOIC	8-Pin Plastic DIP
HT0440LG	HT0440N4

Features

- ☐ ±400V input to output isolation
- ☐ ±700V isolation between outputs
- ☐ No external voltage supply required
- ☐ Dual isolated output drivers
- ☐ Option of internal or external clock

Applications

- ☐ Telecommunications
- ☐ Modems
- ☐ Solid state relays
- ☐ High side switches
- ☐ High end audio switches
- ☐ Avionics
- ☐ ATE

Absolute Maximum Ratings

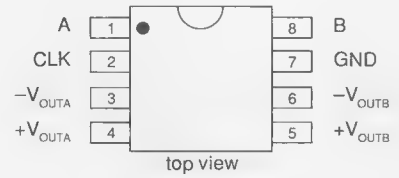
Input to Output Isolation Voltage, V_{ISO}	±400V
Logic Input Voltage, V_A, V_B	–0.5 to +7.0V
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to +150°C

Note: All voltages are referenced to ground.

General Description

The Supertex HT0440 is a dual high voltage isolated driver utilizing Supertex's proprietary HVCMOS® technology. It is designed to drive discrete MOSFETs configured as bidirectional or unidirectional switches. It can drive N-channel MOSFETs as high side switches up to 400V. The HT04 has an internal clock which generates two independent DC isolated voltages to the outputs, V_{OUTA} and V_{OUTB} when logic inputs A and B are at logic high. The internal clock can be disabled by applying an external clock signal to the CLK pin. This allows the power dissipation and AC characteristics to be tailored to meet specific needs. The HT04 does not require any external power supplies. The internal supply voltage is supplied by either of the two logic inputs A or B when they are at logic high.

Pin Configuration



top view

8-pin DIP/SO-8

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Electrical Characteristics

(over recommended operating conditions, T_A = 25°C unless otherwise specified)

DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
I_{IHA}, I_{IHB}	Logic high input current (per input)			500	µA	V_A = 3.5V, V_B = 3.5V, CLK = 0V
				250	µA	V_A = 3.5V, V_B = 3.5V, CLK = 500KHz
				1.0	mA	V_A = 3.5V, V_B = 3.5V, CLK = 2.0MHz
				2.0	mA	V_A = 5.5V, V_B = 5.5V, CLK = 0V
				1.0	mA	V_A = 5.5V, V_B = 5.5V, CLK = 500KHz
V_{OUTA}, V_{OUTB}	Output Voltage	6.0			V	V_A = 3.15V, V_B = 3.15V, CLK = 0V, no load
		5.0			V	V_A = 3.15V, V_B = 3.15V, CLK = 500KHz, no load
		6.0			V	V_A = 3.15V, V_B = 3.15V, CLK = 2.0MHz, no load
		10.0			V	V_A = 4.5V, V_B = 4.5V, CLK = 0V, no load
		8.0			V	V_A = 4.5V, V_B = 4.5V, CLK = 500KHz, no load
I_{ILA}	Logic low input A current			10	µA	V_A = 0.5V, V_B = high
I_{ILB}	Logic low input B current			10	µA	V_A = high, V_B = 0.5V
I_{ILO}	Quiescent current			10	µA	V_A = 0.5V, V_B = 0.5V
V_{ISO}	Input to output isolation voltage	±400			V	
V_{CISO}	Output to output isolation voltage	±700			V	

AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$t_{d(ON)}$	Turn on delay time			50	µs	See timing diagram and test circuit
t_r	Rise time			650	µs	CLK = 0V, C_L = 600pF
$t_{d(OFF)}$	Turn off delay time			150	µs	
t_f	Fall time			3.0	ms	

Recommended Conditions

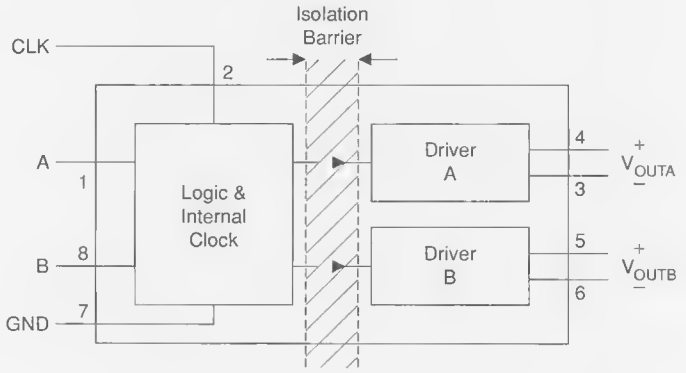
Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CLK	External clock frequency	0.5		2.0	MHz	
V_{IHCLK}	Clock input high voltage	3.15		5.5	V	
V_{ILCLK}	Clock input low voltage	0		0.5	V	
V_{IH}	Logic input high voltage	3.15		5.5	V	
V_{IL}	Logic input low voltage	0		0.5	V	
T_A	Operating temperature	-40		+85	°C	

Truth Table*

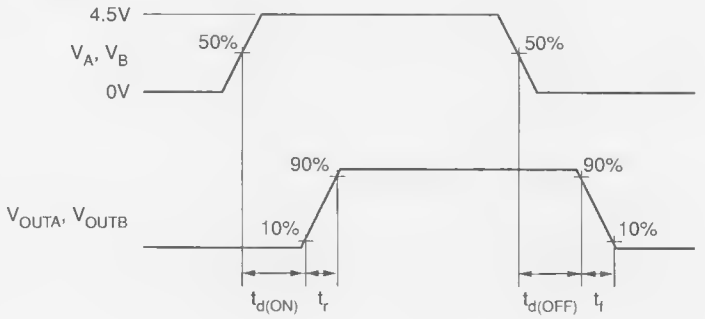
A	B	CLK	$V_{OUT}A$	$V_{OUT}B$	Internal Clock
0	0	0	Off	Off	Off
0	1	0	Off	On	On
1	0	0	On	Off	On
1	1	0	On	On	On
0	0	Clk	Off	Off	Off
0	1	Clk	Off	On	Off
1	0	Clk	On	Off	Off
1	1	Clk	On	On	Off

*CLK pin must be connected to ground when the internal clock is required.

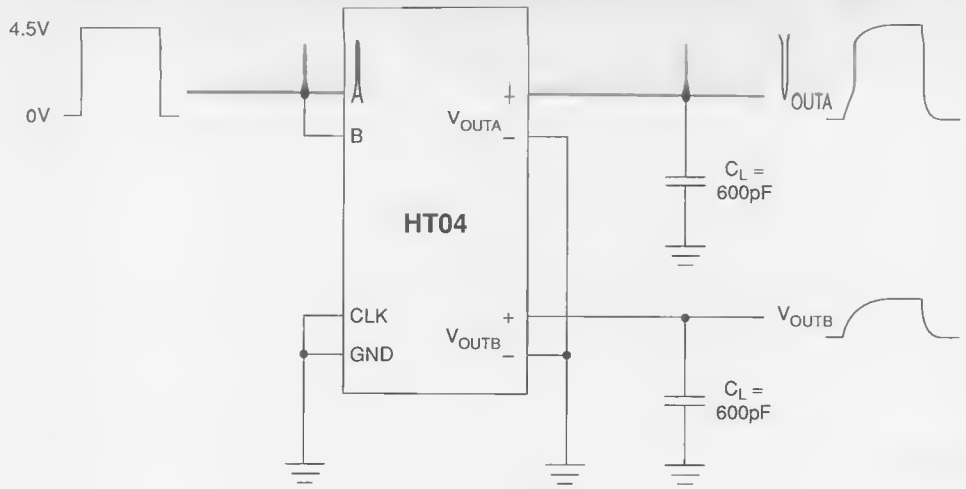
Block Diagram



Timing Diagram



Test Circuit



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